AMENDMENTS TO THE SPECIFICATION

Please amend the specification as follows.

On pages 4-5, paragraph [0013]:

In some aspects, the invention relates to an apparatus for simulating ~~modeling~~ an anti-resonance circuit of a microprocessor, including ~~comprising:~~ a simulated load model ~~that simulates the anti-resonance circuit;~~, a simulated transistor that simulates at least one high frequency capacitance of the anti-resonance circuit, ~~capacitor,~~ where[[in]] the simulated transistor is connected in parallel with the simulated load model; and a simulated capacitor that simulates an intrinsic capacitance of a section of the microprocessor, where[[in]] the simulated capacitor is connected in parallel with the simulated load model.

On page 5, paragraph [0014]:

In other aspects, the invention relates to a method ~~an apparatus~~ for simulating ~~modeling~~ an anti-resonance circuit of a microprocessor, including ~~comprising: means for simulating an anti-resonance circuit; and means for synchronizing the means for simulating an anti-resonance circuit with a clock signal~~ simulating a load of the anti-resonance circuit, simulating at least one high-frequency capacitance in parallel with the simulated load, and simulating a section of the microprocessor's intrinsic capacitance in parallel with the simulated load.

On page 5, paragraph [0015]:

In other aspects, the invention relates to an apparatus ~~method~~ for modeling an anti-resonance circuit of a microprocessor, including a processor, memory, and instructions residing in the memory and executable by the processor to simulate ~~comprising: modeling~~ a load ~~to generate a simulation~~ of [[an]]the anti-resonance circuitwith a simulated resistor,~~; simulating~~ simulate a ~~at least one~~ high frequency capacitance of the anti-resonance circuit with a simulated transistor connected ~~capacitor~~ in parallel with the simulated resistor, ~~load model;~~ and simulate an ~~simulating a section of the microprocessor's~~ intrinsic capacitance in parallel with the simulated resistor~~load model~~.